

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	184	703/14.ccls. and @pd>"20060301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/12/26 11:05

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	58	((mixed near signal) or mixed-signal) near simulation	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/12/26 11:23
L5	57	((analog near digital) or analog-digital or digital-analog) near simulation	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/12/26 11:24

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	12	biput	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/12/26 11:49

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L11	11	(bidirectional adj node\$1) and simulat\$4	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/12/26 11:52

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Results 1 - 10 of about 124 for input. (0.06 seconds)

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Did you mean: **input**

[M Samatham](#)

[G Niemeyer](#)

[D Hanna](#)

[L Svensson](#)

[P Enjeti](#)

Voltage level translation for an output driver system with a bias generator - group of 2 »

F Hinedi, M Cases, S Dutta, RH Dennard - US Patent 5,986,472, 1999 - Google Patents

... A gate of transistor 118 is connected to bias circuit 130 at Node E. A drain of transistor 118 is connected to an information node **IOPUT**, which is connected to ...

[Cited by 7](#) - [Related Articles](#) - [Web Search](#)

Stacked PFET off-chip driver with a latch bias generator for overvoltage protection - group of 2 »

F Hinedi, L Mamileti - US Patent 6,141,200, 2000 - Google Patents

... **GND IOPUT** Page 2. ... multiply/add operations, and includes floatingpoint registers output terminal **IOPUT**. 120 performs single precision and/or double precision ...

[Related Articles](#) - [Web Search](#)

Discrete adaptive control: A sufficient condition for stability and applications - group of 3 »

JJ Fuchs - Automatic Control, IEEE Transactions on, 1980 - [ieeexplore.ieee.org](#)

... **we-ioput** singleoutput systems is considered using a model-reference type approach. A sufficient condition upon the adaptation mechanism is obtained Any ...

[Cited by 5](#) - [Related Articles](#) - [Web Search](#)

Concurrent Hierarchical and Multilevel Simulation of VLSI Circuits - group of 3 »

RB Mueller-Thuns, JT Rahmeh, JA Abraham, JA Wehbeh ... - SIMULATION, 1993 - [sim.sagepub.com](#)

Page 1. 79 TECHNICAL ARTICLE Concurrent Hierarchical and Multilevel Simulation of VLSI Circuits & dagger; Robert B. Mueller-Thuns Cadence Design System Inc. ...

[Related Articles](#) - [Web Search](#) - [BL Direct](#)

Circuit and method for voltage level translation utilizing a bias generator - group of 2 »

F Hinedi, M Cases, S Dutta, RH Dennard - US Patent 5,867,010, 1999 - Google Patents

... the art. Resistor 110 couples clamp device 102 to an external signalling device via signal pad input, **IOPUT**, 112. Diode devices ...

[Cited by 4](#) - [Related Articles](#) - [Web Search](#)

The de Bruijn multiprocessor network: a versatile parallel processing and sorting network for VLSI - group of 8 »

MR Samatham, DK Pradhan - IEEE Transactions on Computers, 1989 - [doi.ieeecomputersociety.org](#)

... input/sequential output, 2) parallel input/sequential output, 3) parallel inputparallel output, 4) sequential input¶llel output, 5) hybrid **ioput**/l@rid ...

[Cited by 124](#) - [Related Articles](#) - [Web Search](#)

Performance in adaptive manipulator control - group of 5 »

G Niemeyer, JJE Slotine - Decision and Control, 1988., Proceedings of the 27th IEEE ..., 1988 - [ieeexplore.ieee.org](#)

... Li and Slotine, 1988], [Walker, 1988]), and led to the remarkable result that global convergence properties similar to those of single-**ioput** linear systems can ...

[Cited by 39](#) - [Related Articles](#) - [Web Search](#)

AIDE-A Tool for Computer Architecture Design - group of 2 »

DJ Ellenberger, YW Ng - Design Automation, 1981. 18th Conference on, 1981 - [ieeexplore.ieee.org](#)

... The description begins with a type name for the module, followed by declarations of all inputs and outputs (an **ioput** functions as both). ...

[Cited by 3](#) - [Related Articles](#) - [Web Search](#)

Continuous-wave oscillation of a monomode ytterbium-doped fiber laser - group of 4 »

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Results 1 - 10 of about 11 for **input mixed signal**. (0.07 seconds)

All Results

[R Chadha](#)

[D Saab](#)

[C Chen](#)

[C Visweswariah](#)

[R Mueller-Thun...](#)

Did you mean: **[kaputa mixed signal](#)**

[Design methodology and simulation tools for mixed analog-digital integrated circuits](#)

R Beale, R Chadha, CF Chen, A Prosser, KM Tham - Circuits and Systems, 1990., IEEE International Symposium on, 1990 - [ieeexplore.ieee.org](#)

... and digital behavior. Although an integrated **mixed** AD simulator is a major tool for **mixed signal** designs. the design cost cannot ...

[Cited by 1](#) - [Related Articles](#) - [Web Search](#)

[Hierarchical mixed-level simulation of VHDL descriptions](#)

T Karnik, DG Saab, SM Kang, YK Lee, KH Kim - ASIC Conference and Exhibit, 1994. Proceedings., Seventh ..., 1994 - [ieeexplore.ieee.org](#)

... characteristics of these circuits, such as, bidirectional **signal** flow, ratioed ... INPUT, OUTPUT or bidirectional **IOPUT**. ... Figure 4 illustrates a **mixed-level** circuit. ...

[Web Search](#)

[M 3-a multilevel mixed-mode mixed A/D simulator - group of 4 »](#)

R Chadha, C Visweswariah, CF Chen - Computer-Aided Design of Integrated Circuits and Systems, ..., 1992 - [ieeexplore.ieee.org](#)

... 5. MAY 1992 575 0278-0070/92\$03.00 © 1992 IEEE M3-A Multilevel **Mixed-Mode Mixed** A/D Simulator Rakesh Chadha, Senior Member, IEEE, Chandramouli Visweswariah ...

[Cited by 8](#) - [Related Articles](#) - [Web Search](#)

[Concurrent Hierarchical and Multilevel Simulation of VLSI Circuits - group of 3 »](#)

RB Mueller-Thuns, JT Rahmeh, JA Abraham, JA Wehbeh ... - SIMULATION, 1993 - [sim.sagepub.com](#)

... The program allows for user-supplied behavioral models, assignable delays, and bidirectional **signal** flow inside circuit blocks that are represented as ...

[Related Articles](#) - [Web Search](#) - [BL Direct](#)

[Analogue IF beamformers](#)

NJ Easton, FC Bennett, CW Miller - Multiple Beam Antennas and Beamformers, IEE Colloquium on, 1989 - [ieeexplore.ieee.org](#)

... coming from the individual antenna elements is **mixed** with the ... Thus if the **signal** is split into four orthogonal ... At each node where the **input** and output lines ...

[Web Search](#)

[FREQUENCY SYNTHESIS SYSTEM](#)

FL PUTZRATH - US Patent 2,797,326, 1957 - Google Patents

... delay provided thereby, a frequency f_i different from the **input** frequency f_o ... that if f_o and f_i are modulated or **mixed** together, the resultant **signal** will be ...

[Cited by 1](#) - [Related Articles](#) - [Web Search](#)

[Hierarchical multi-level fault simulation of large systems - group of 3 »](#)

DG Saab, RB Mueller-Thuns, D Blaauw, JT Rahmeh, JA ... - Journal of Electronic Testing, 1990 - Springer

... 3. It allows **mixed-mode** simulation: parts of the ... circuit, we introduce a bidirectional type (denoted **IOPUT**). ... captures the notion of bidirectional **signal** flow and ...

[Cited by 14](#) - [Related Articles](#) - [Web Search](#)

[Fault grading of large digital systems](#)

DG Saab, RB Mueller-Thuns, D Blaauw, JT Rahmeh, JA ... - Computer Design: VLSI in Computers and Processors, 1990. ..., 1990 - [ieeexplore.ieee.org](#)

... It allows **mixed** mode simulation: parts of the ... a subcircuit, we introduce a bidirectional type (denoted **IOPUT**). ... Captures the notion of bidirectional **signal** flow and ...

[Related Articles](#) - [Web Search](#)

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	12	ioput	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/12/26 11:43

Scholar

Results 1 - 3 of 3 for **input digital-analog**. (0.06 seconds)

All Results

Did you mean: **input** digital-analog

[R Chadha](#)

[C Chen](#)

[C Visweswariah](#)

[M Andrews](#)

[S Khanna](#)

Design methodology and simulation tools for mixed analog-digitalintegrated circuits

R Beale, R Chadha, CF Chen, A Prosser, KM Tham - Circuits and Systems, 1990., IEEE International Symposium on, 1990 - [ieeexplore.ieee.org](#)

... A generic top-down, bottom-up design methodology is described which allows **digital**, **analog** and mixed AD portions of the circuit to be specified at various ...

[Cited by 1](#) - [Related Articles](#) - [Web Search](#)

M 3-a multilevel mixed-mode mixed A/D simulator - group of 4 »

R Chadha, C Visweswariah, CF Chen - Computer-Aided Design of Integrated Circuits and Systems, ..., 1992 - [ieeexplore.ieee.org](#)

... Thus, the methodology allows **digital**, **analog**, and mixed analog/digital subcircuits to be described at various levels, among them the behavioral, functional ...

[Cited by 8](#) - [Related Articles](#) - [Web Search](#)

Integrated scheduling of unicast and multicast traffic in aninput-queued switch - group of 7 »

M Andrews, S Khanna, K Kumaran - INFOCOM'99. Eighteenth Annual Joint Conference of the IEEE ..., 1999 - [ieeexplore.ieee.org](#)

... A label in a slot implies that a multicast packet is scheduled there. The label denotes the **input** port where the packet arrived. ...

[Cited by 27](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Did you mean to search for: **input** digital-analog

input digital-analog

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Results 1 - 2 of 2 for **input analog-digital**. (0.05 seconds)

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[R Chadha](#)

[C Chen](#)

[C Visweswariah](#)

Did you mean: **input** analog-digital

M 3-a multilevel mixed-mode mixed A/D simulator - group of 4 »

R Chadha, C Visweswariah, CF Chen - Computer-Aided Design of Integrated Circuits and Systems, ..., 1992 - [ieeexplore.ieee.org](#)

... Chin-Fu Chen, Member, IEEE Abstract—This paper describes a unified multilevel mixed-mode simulation capability for mixed **analog/digital** integrated circuits. ...

[Cited by 8](#) - [Related Articles](#) - [Web Search](#)

Design methodology and simulation tools for mixed analog-digital integrated circuits

R Beale, R Chadha, CF Chen, A Prosser, KM Tham - Circuits and Systems, 1990., IEEE International Symposium on, 1990 - [ieeexplore.ieee.org](#)

Page 1 Design Methodology and Simulation Tools for Mixed **Analog-Digital** Integrated Circuits CH2868-8/90/OOOI\$() © 1990 IEEE Richard Beale, Rakesh Chadha, Chin ...

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Results 1 - 1 of 1 for ioput mixed-signal. (0.04 seconds)

Did you mean: **kaputa** mixed-signal

Design methodology and simulation tools for mixed analog-digitalintegrated circuits

R Beale, R Chadha, CF Chen, A Prosser, KM Tham - Circuits and Systems, 1990., IEEE International Symposium on, 1990 -
ieeexplore.ieee.org

... analog and digital behavior. Although an integrated mixed AD simulator
is a major tool for **mixed signal** designs. the design cost ...

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
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- ☐ **1. AIDE - A Tool for Computer Architecture Design**
 Ellenberger, D.J.; Ng, Y.W.;
Design Automation, 1981, 18th Conference on
 29-1 June 1981 Page(s):796 - 803
[Abstract](#) | Full Text: [PDF\(672 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ **2. On-Line Simulation of Block-Diagram Systems**
 Dertouzos, M.L.; Kaliski, M.E.; Polzen, K.P.;
Computers, IEEE Transactions on
 Volume C-18, Issue 4, April 1969 Page(s):333 - 342
[Abstract](#) | Full Text: [PDF\(2008 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **3. The Open Channel**
 Burkhardt, W.H.; Yuen, C.K.;
Computer
 Volume 17, Issue 9, Sept. 1984 Page(s):119 - 120
[Abstract](#) | Full Text: [PDF\(2136 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **4. Implementation of a fast digital processor using the residue number system**
 Chao Huang; Peterson, D.; Rauch, H.; Teague, J.; Fraser, D.;
Circuits and Systems, IEEE Transactions on
 Volume 28, Issue 1, Jan 1981 Page(s):32 - 38
[Abstract](#) | Full Text: [PDF\(992 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **5. On cross coupling and stability in nonlinear control systems**
 Rootenberg, J.; Oso, J.;
Automatic Control, IEEE Transactions on
 Volume 16, Issue 1, Feb 1971 Page(s):73 - 75
[Abstract](#) | Full Text: [PDF\(344 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **6. Criteria for stability of a class of multiplicative nonlinear systems**
 Satyanarayana, N.; Srinath, M.;
Automatic Control, IEEE Transactions on
 Volume 16, Issue 1, Feb 1971 Page(s):75 - 76
[Abstract](#) | Full Text: [PDF\(280 KB\)](#) IEEE JNL
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- 7. A note on Lyapunov type controllers**

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» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard



1. **Fast functional simulation: an incremental approach**

Hwang, S.Y.; Blank, T.; Choi, K.;

[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)

Volume 7, Issue 7, July 1988 Page(s):765 - 774

Digital Object Identifier 10.1109/43.3947

[AbstractPlus](#) | Full Text: [PDF\(984 KB\)](#) IEEE JNL

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X Huang

W Zhang

S HWANG

F Bimbot

T BLANK

Fast Functional Simulation: An Incremental Approach - group of 4 »

SUNY HWANG, TOM BLANK, K CHOI - IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN, 1988 -
ieeexplore.ieee.org

... A port can be input, output, or **biput** (bidirectional). ... b) If the port is an output
or **biput** port: The merged node is directly affected by the

Cited by 14 - Related Articles - Web Search

Generic interactive device model wrapper - group of 2 »

US Patent 5,784,594, 1998 - freepatentsonline.com

... device interface. 4. The method of claim 1 wherein said interface pins include
input pins, output pins and **biput** pins. 5. The method ...

Cited by 3 - Related Articles - Cached - Web Search

Transistor-level timing and simulator and power analyzer - group of 2 »

X Huang, WH Zhang - US Patent 5,553,008, 1996 - Google Patents

Page 1. United States Patent Huang et al. US005553008A [li] Patent Number: [45]

Date of Patent: [54] TRANSISTOR-LEVEL TIMING AND SIMULATOR AND POWER ANALYZER ...

Cited by 57 - Related Articles - Web Search

Transistor-level timing and power simulator and power analyzer - group of 3 »

X Huang, WH Zhang - US Patent 5,446,676, 1995 - Google Patents

Page 1. United States Patent Huang et al. [54] TRANSISTOR-LEVEL TIMING AND
POWER SIMULATOR AND POWER ANALYZER [75] Inventors: Xiaoli ...

Cited by 35 - Related Articles - Web Search

Variable-length sequence modeling: multigrams - group of 2 »

F Bimbot, R Pieraccini, E Levin, B Atal - Signal Processing Letters, IEEE, 1995 - ieeexplore.ieee.org

... Page 2 **biput** text 1 blessedlstheafththatWalkethnbumnt00ueb0ftheg001ta

ndeth1ntheWayOfSifflerSn0r51ttetfhnt5e5eat0tt05tf 2 buthisdelightistnthe1aWOrth ...

Cited by 28 - Related Articles - Web Search

Current-mode band-pass filters with Q-magnification - group of 2 »

A Fabre, H Amrani, O Saaïd - Circuits and Systems II: Analog and Digital Signal ..., 1996 -
ieeexplore.ieee.org

Page 1 00a 0 * N' N' * Nt N' *)NN' 0..ooo 0000 * 0 * N' N' 0 0 0

UUU IC ** 0 C 1.5 3 25 3 **biput** cup.,? mA (a) — N' B ...

Cited by 7 - Related Articles - Web Search - BL Direct

Optimal set placement and multidimensional fuzzy sets for fuzzylogic controllers - group of 3 »

GT Foster, C Khambhampati - Control, 1994. Control'94. Volume 1., International ..., 1994 -
ieeexplore.ieee.org

... The advantage of this approach is a reduction in the number of rules required
to represent a non-linear multi-**biput** control scheme. ...

Cited by 4 - Related Articles - Web Search - BL Direct

Surface-Normal Modulation and Switches

C Table, C Specifications - IEEE J. Select. Areas Commun, 1994 - ieeexplore.ieee.org

... Page 2 **biput** rittcduu Implanted flPtAu.In Content Th'eltenducInImtk 'mfleror

,WjW// J'//J/, - The wavelength dependence of am- plification for ...

Web Search

Circuit analyzer of black, gray and transparent elements - group of 5 »

J Avidan - US Patent 6,158,022, 2000 - Google Patents

Scholar All articles Recent articles

Results 1 - 10 of about 5,360 for **bidirectional node simulation**. (0.17 seconds)

All Results

C Perkins

E Royer

J Broch

D Maltz

D Johnson

Ad-hoc on-demand distance vector routing - group of 125 »

CE Perkins, EM Royer - 1999 - doi.ieeecomputersociety.org

... the RREQ was received over a **bi-directional** link. ... to ensure that only **nodes** with **bidirectional** connectivity are ... creates a session to another **node** selected at ...

Cited by 3874 - Related Articles - Web Search

[BOOK] COSMOS: a compiled simulator for MOS circuits - group of 2 »

RE Bryant, D Beatty, K Brace, K Cho, T Sheffler - 1987 - ACM Press New York, NY, USA

Cited by 163 - Related Articles - Web Search - Library Search

A performance comparison of multi-hop wireless ad hoc network routing protocols - group of 86 »

J Broch, DA Maltz, DB Johnson, YC Hu, J Jetcheva - Proceedings of the 4th annual ACM/IEEE international ..., 1998 - portal.acm.org

... implementation [23], was included in the **simulation** and used ... DSR to discover ordy routes composed of **bidirectional** finks by requiring that a **node** return rdl ...

Cited by 1891 - Related Articles - Web Search

MOSSIM: A Switch-Level Simulator for MOS LSI - group of 3 »

RE Bryant - Design Automation, 1981. 18th Conference on, 1981 - ieeexplore.ieee.org

... of the network into a set of transistor groups prior to **simulation**. Each group contains a set of **nodes** and transistors with **bidirectional** connections. ...

Cited by 47 - Related Articles - Web Search - Library Search

Method and apparatus for optimizing computer networks - group of 3 »

M Liron - US Patent 5,598,532, 1997 - Google Patents

... 221 Determine **Bidirectional** Cost of Traffic for ... collectors 17, consolidator 25, **simulator** 37, and ... 6 is a pictorial illustration of **bi-directional node to node** ...

Cited by 50 - Related Articles - Web Search

On the reduction of broadcast redundancy in mobile ad hoc networks - group of 2 »

W Peng, XC Lu - Proceedings of the 1st ACM international symposium on Mobile ..., 2000 - portal.acm.org

... The **simulation** results show that broadcast redundancy can be ... antenna is used and all mobile **nodes** have the ... So, there exists a **bi-directional** link between two ...

Cited by 177 - Related Articles - Web Search

Mitigating routing misbehavior in mobile ad hoc networks - group of 52 »

S Marti, TJ Giuli, K Lai, M Baker - Proceedings of the 6th annual international conference on ..., 2000 - portal.acm.org

... path to send back the reply (**bidirectional** links are ... in our simulations since the cur- rent **simulation** period is too short to reset a misbehaving **node's** rating ...

Cited by 622 - Related Articles - Web Search

The Second Generation MOTIS Mixed-Mode Simulator - group of 2 »

CF Chen, CY Lo, HN Nham, P Subramaniam - Design Automation, 1984. 21st Conference on, 1984 - ieeexplore.ieee.org

... into normal gates are modeled as **bi-directional** transmission gates. ... as the number of **bidirectional** components in ... of 3 phases, namely, **node** initialization, **node** ...

Cited by 26 - Related Articles - Web Search

IRSIM: An Incremental MOS Switch-Level Simulator - group of 3 »

A Salz, M Horowitz - Design Automation, 1989. 26th Conference on, 1989 - ieeexplore.ieee.org

... an event-driven, switch-level **simulator** that represents a ... **Nodes** are wires that are modeled as capacitors ... sistors are modeled as **bidirectional** switches; turning ...